

FIG.1

1 RECEIVING APPARATUS

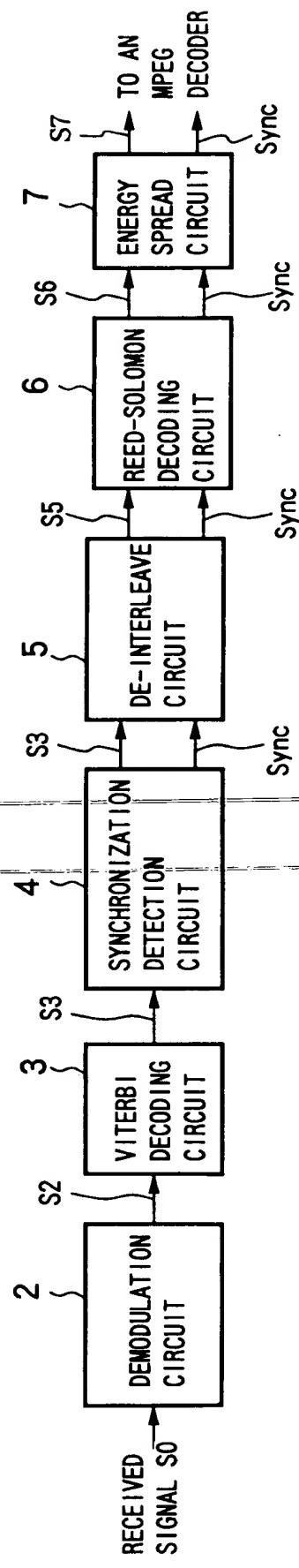
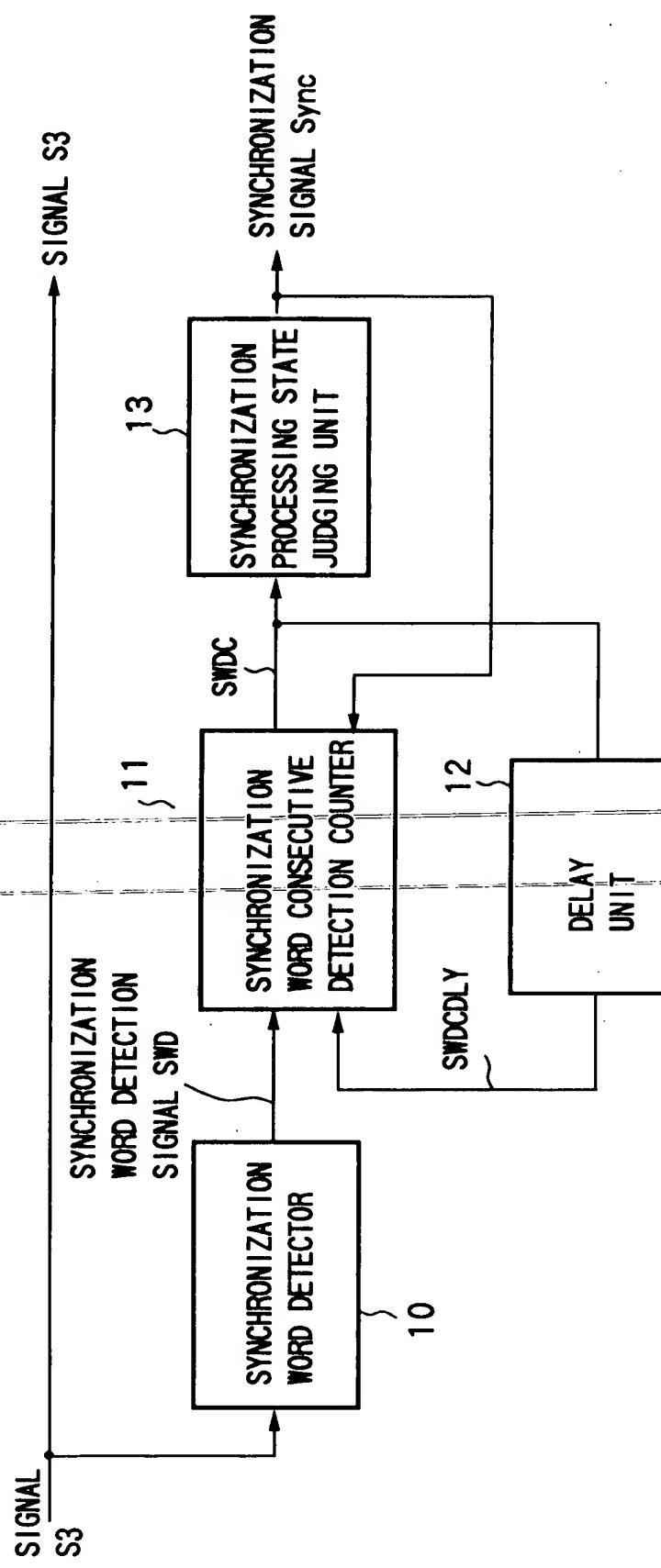
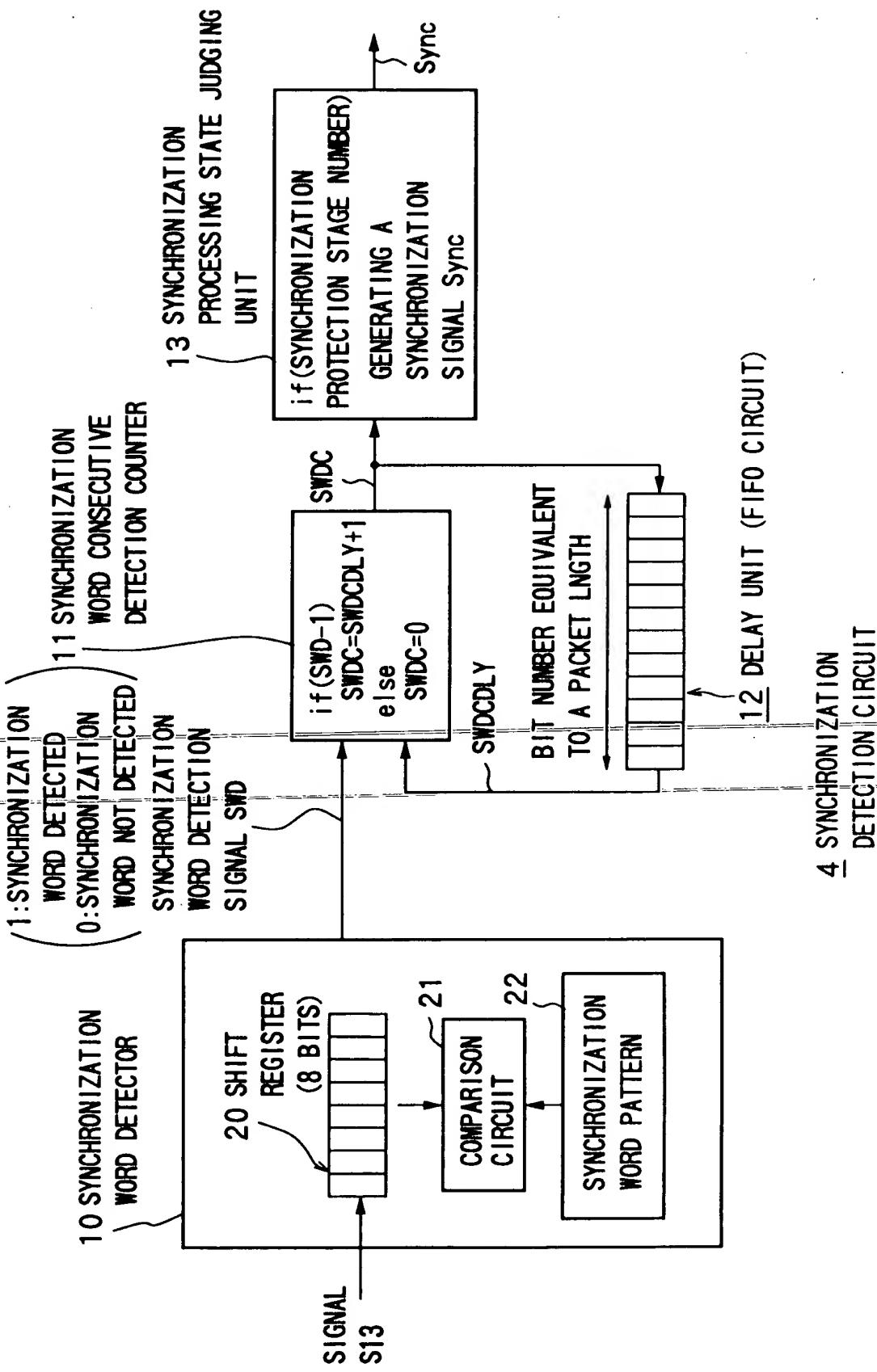


FIG.2



4 SYNCHRONIZATION
DETECTION CIRCUIT

FIG.3



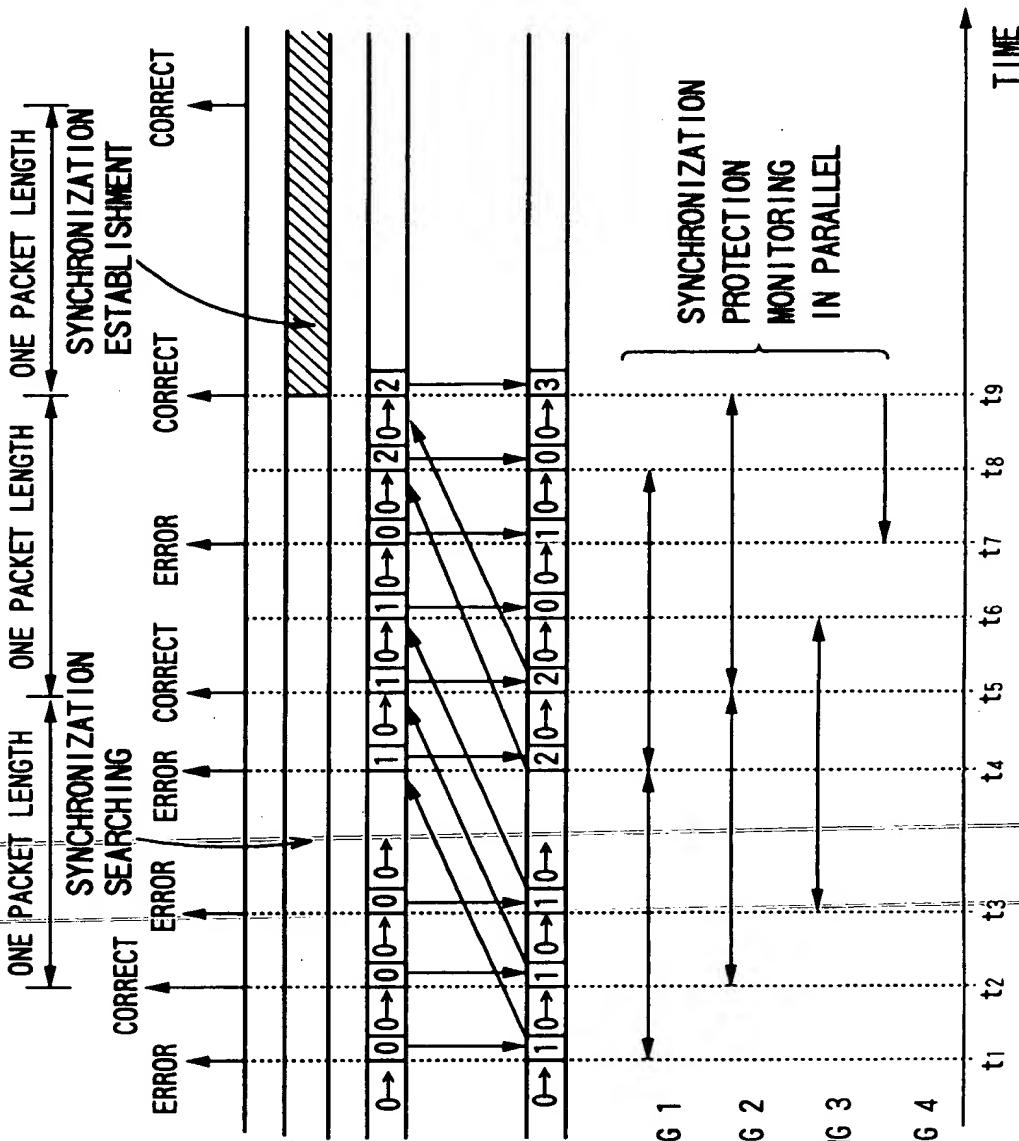
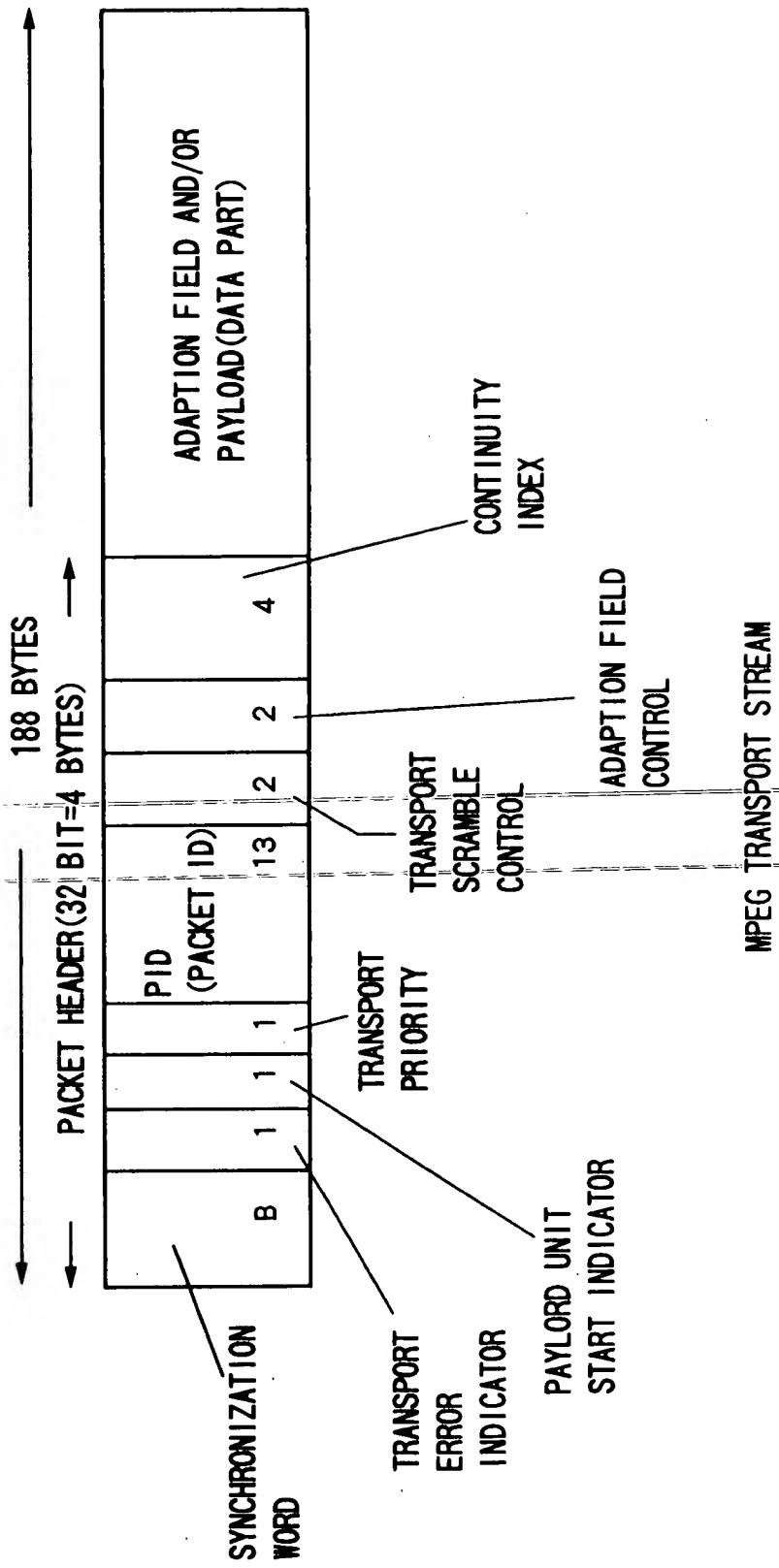


FIG.5



00000 = 100000000000

FIG.6A TRANSPORT
STREAM PACKET

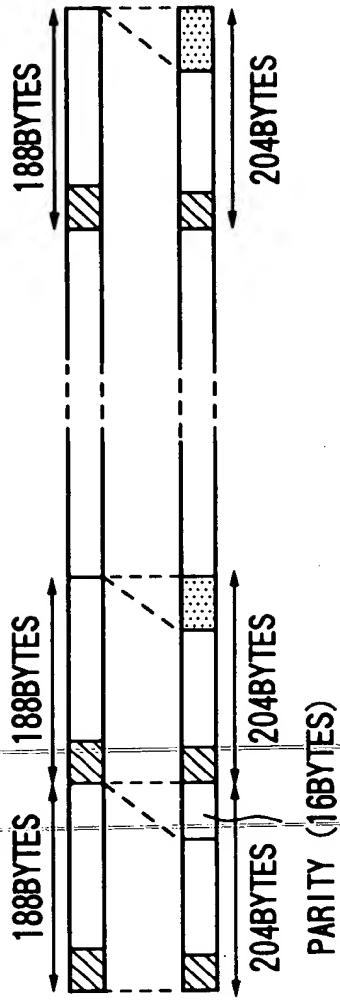
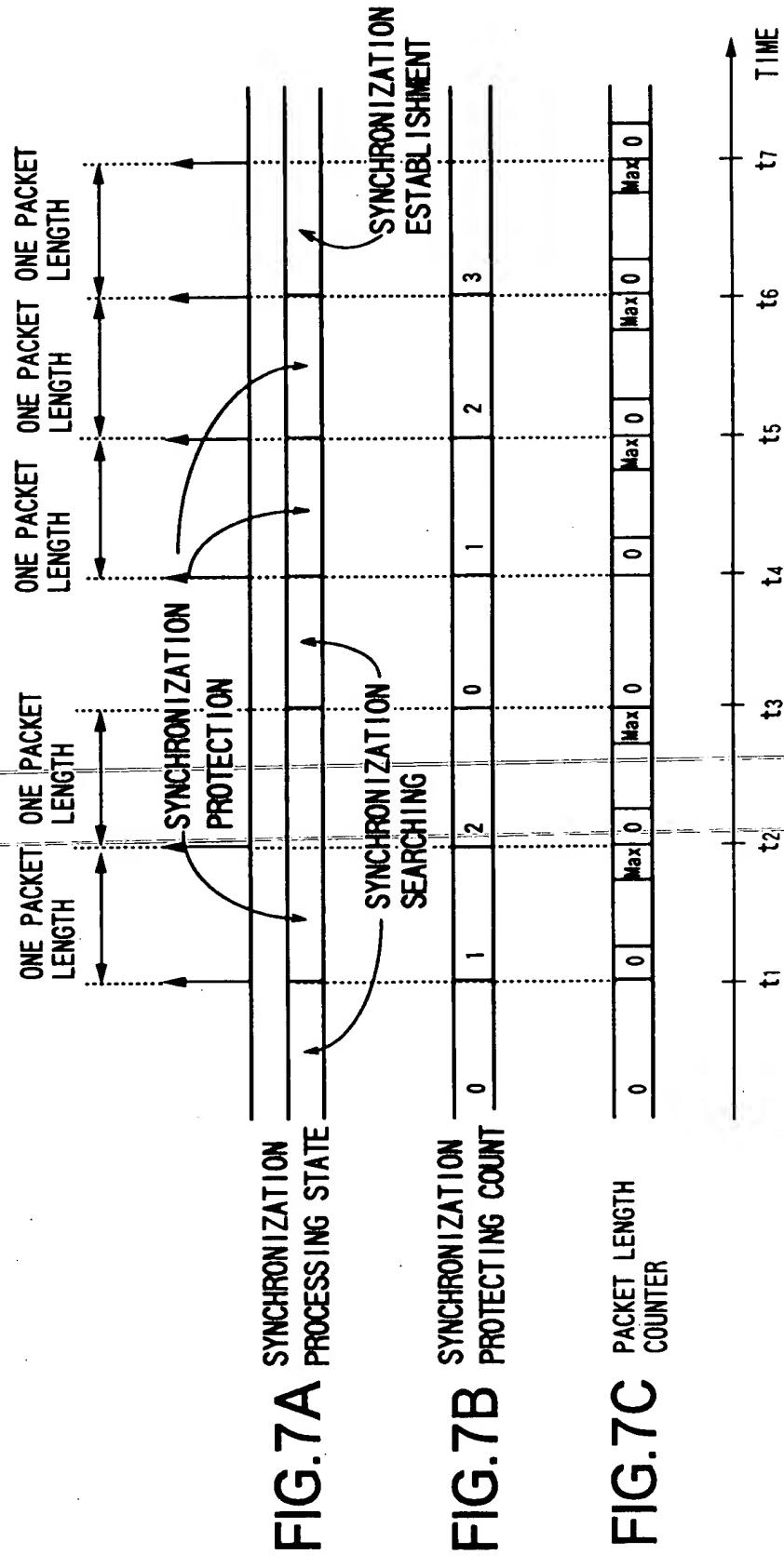


FIG.6B SLOT DATA



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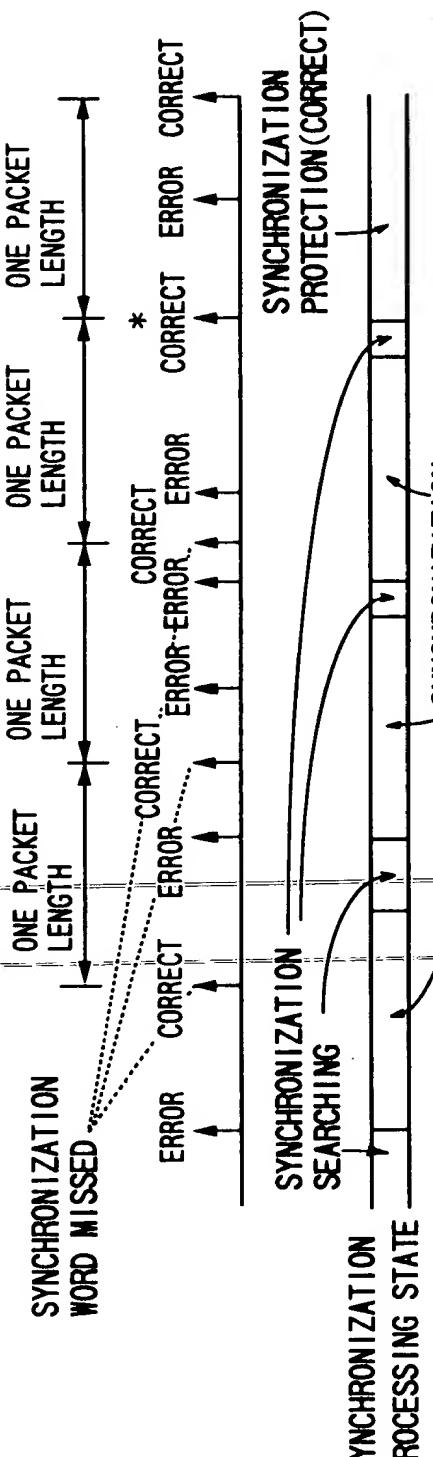
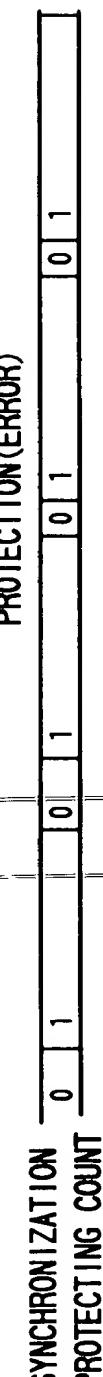


FIG. 8A



EIG. 8

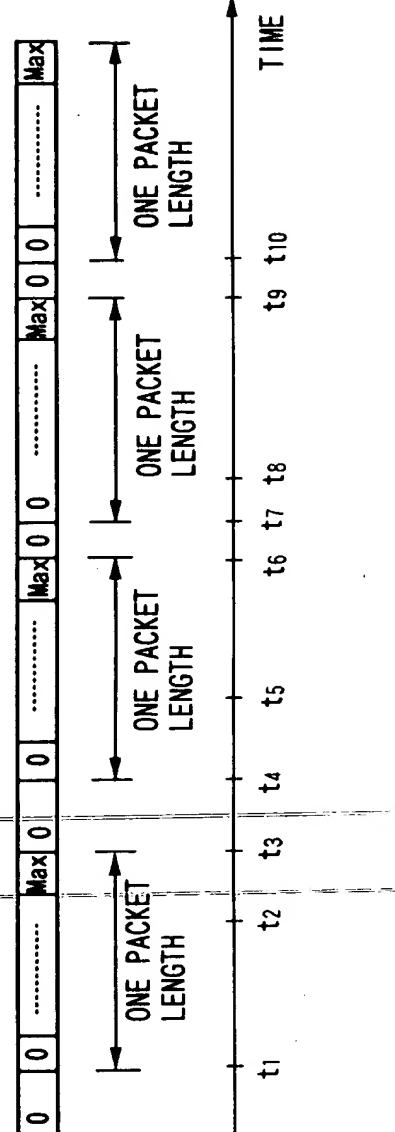


FIG. 8C